



FL2010 USB3.2 Communication Module User Manual

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Document revision history

chapter	Revision Overview
V 1.0	
all	First version released

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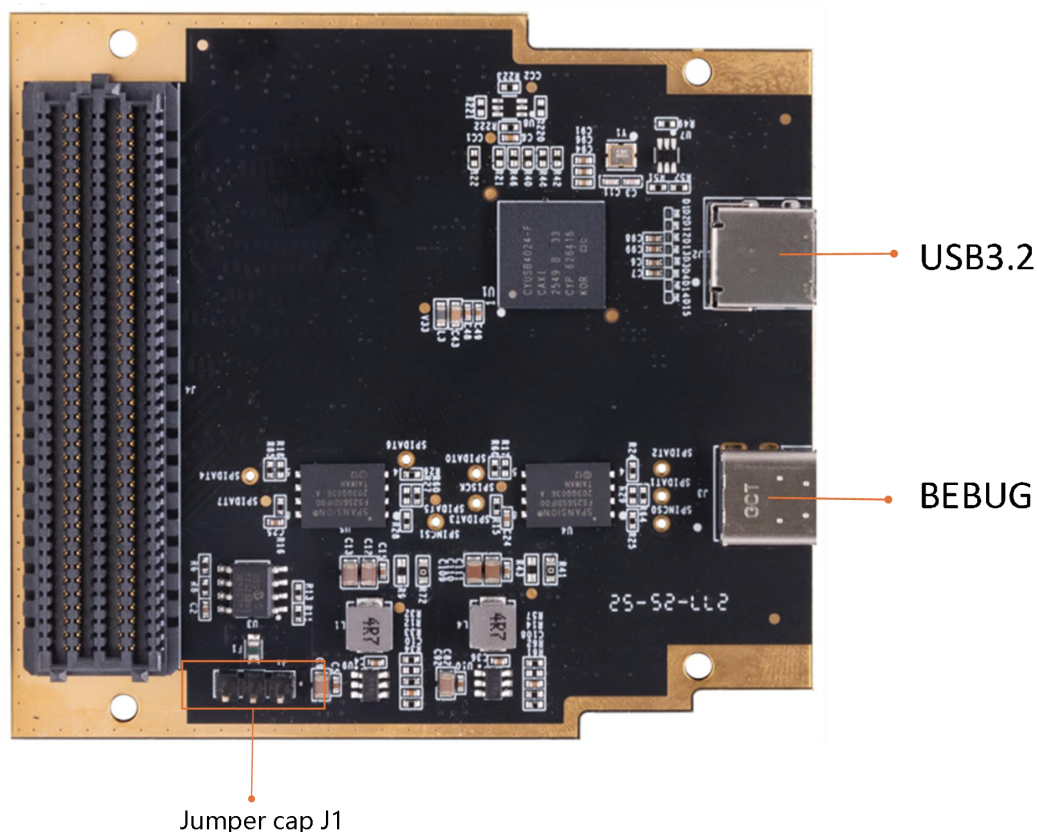
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Chapter1 USB 3.2 Module Introduction

This document is the user manual for the "USB 3.2 High-Speed Communication Module FMC Card" . It details the card's main functions, performance specifications, interface descriptions , hardware connection instructions, program usage instructions, and programming steps . This document serves as the user 's primary reference manual, providing guidance for secondary development and also acting as a selection reference.

1.1 Overview

This FMC card uses the Infineon EZ-USB FX20 as its USB host controller chip, with a maximum uplink speed of 20Gbps. The EZ-USB FX20 is a highly integrated chip, internally integrating a Cortex-M4 ARM architecture processor, a USB driver unit, and on-chip FLASH memory. This FMC card has two USB Type-C interfaces: one low-speed USB 2.0 interface for printing serial data; and the other a high-speed USB 3.2 interface for transmitting high-speed data. This module conforms to the FMC-LPC interface specification and interacts with the FPGA FMC card via an LVDS differential link. A picture of the FL2010 module is shown below :



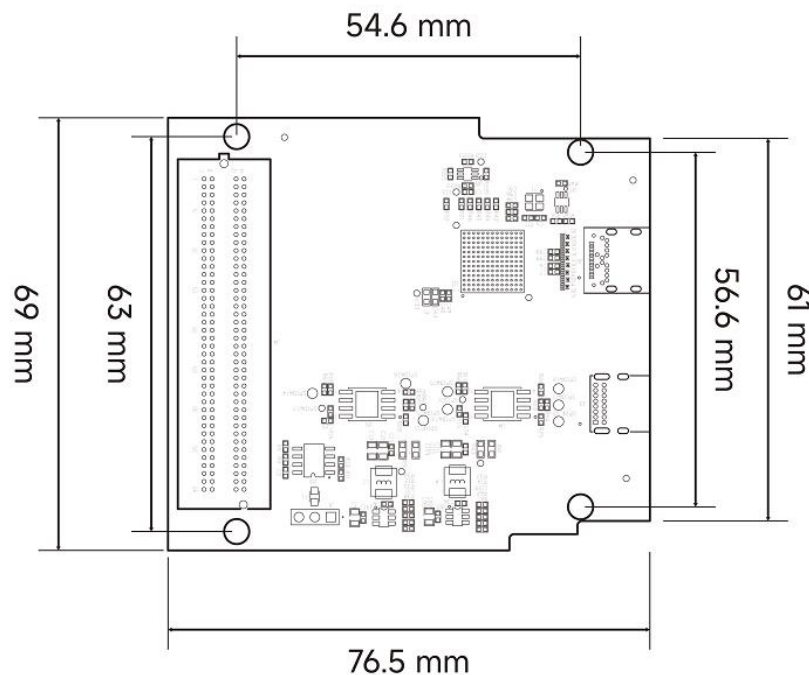
- The two pins on the left form the FMC interface, supplying power to the module.
- The two pins on the right form the USB interface, supplying power to the module (for use when the module is not connected to an FPGA development board).

1.2 Key Performance Indicators

The following are the detailed specifications of this product:

- USB 3.2 conversion chip: Equipped with one Infineon EZ-USB FX20 chip, model number CYUSB4024;
- USB 3.2 transmission channels: 1;
- USB serial port debugging channel: 1 channel;
- USB 3.2 theoretical operating speed: 20Gbps;
- FMC Interface Type: LPC (Low Pin Count);
- Digital interface level standard: LVDS (Low-Voltage Differential Signaling) level standard;
- Operating temperature range: $-40^{\circ}\text{C} \sim 85^{\circ}\text{C}$.

1.3 Structural Dimensions



1.4 Installation and Use

The FL2010 is a standard FMC card that can be used on FPGA carrier board with FMC interfaces that conform to the VITA 57.1 specification.

The FL2010 module uses three DC power supplies—3.3V, 1.2V, and VADJ—provided via the FMC connector. The module supports a VADJ voltage range of 1.65V to 3.3V; considering the LVDS data communication requirements of the FPGA development board, a typical VADJ operating voltage of 2.5V or 1.8V is recommended.

The FL2010 communicates with the baseboard via LVDS signals, while the board's control and

trigger signals are at LVCMOS levels, with the level standard determined by the VADJ power supply voltage.

The jumper cap J1 on the FL2010 module is used to switch the module's power supply, providing two selectable modes:

- Default mode: The FMC interface supplies power to the module.
- Optional mode: Power the module via USB interface (for scenarios where the module is not connected to an FPGA development board).

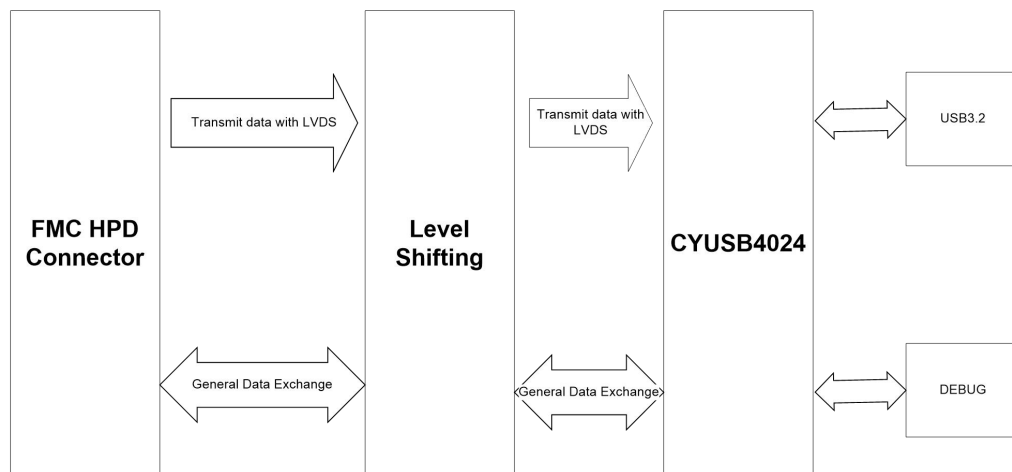
When switching modes, the power must be turned off first to avoid damaging the module by hot-plugging the jumper cap. The jumper cap is for shorting and must be firmly inserted to avoid unstable power supply due to poor contact.

When installing the circuit board, operators should take precautions against electrostatic discharge (ESD). Without ESD protection, do not directly touch the circuit board components.

Chapter2 Function Description

2.1 FL2010 Module Schematic Diagram

The FL2010 module uses the EZ-USB™ FX20 (CYUSB4024) USB 3.2 controller as the main controller and communicates with the FPGA baseboard through the FMC LPC interface. The overall signal flow and functional module description are as follows:



High-speed data path (LVDS)

The main control chip provides two independent LVDS communication channels, PORT 0 and PORT 1, which are directly connected to the FMC LPC interface. Each channel contains 10 pairs of LVDS differential signals, consisting of 8 pairs of data signals, 1 pair of clock signals, and 1 pair of control signals. The two channels support resource multiplexing and can be combined into 16 pairs of LVDS data bit, effectively improving data transmission bandwidth. Signals are transmitted bidirectionally between the main control chip and the FMC through the LVDS RX/LVCOMS PORT 0/PORT 1 interface.

Control and configuration path (I2C & GPIO)

The module has a total of 3 I2C signals and GPIO signals, which are connected to the FMC LPC interface after passing through a level conversion chip:

P0 I2C: Independent control signal for PORT 0 channel;

P1 I2C: Independent control signal for PORT 1 channel;

Control I2C: Global chip control signal used for master controller configuration and status management;

GPIO: General purpose control signals, which can be converted into additional control functions.

Backend Interface

USB 3.2: 20Gbps transfer rate, serving as a high-speed data exchange interface between the main controller and the host computer;

Debug: Outputs the main control's running status via serial port information for debugging and troubleshooting.

Note: For the specific circuit design, register configuration and electrical characteristics of the CYUSB4024 chip, please refer to its official chip datasheet.

2.2 FMC Interface Description

Pin Number	PIN Name	Signal Name	Description
C10	LA06_P	P1D4P	P1 Channel 4 Data Signal - P
C11	LA06_N	P1D4N	P1 Channel 4 Data Signal -N
C15	LA10_N	FMC_P0CTL4	P0 General Data Signal
C18	LA14_P	FMC_P0CTL0	P0 General Data Signal
C19	LA14_N	FMC_P0CTL1	P0 General Data Port
C22	LA18_P_CC	FMC_P0CTL5	P0 General Data Port
C23	LA18_N_CC	FMC_P0CTL6	P0 General Data Port
C26	LA27_P	FMC_GPIO5	GPIO5 signal
C27	LA27_N	FMC_SWDRST_P11	
D8	LA01_P_CC	P1CP	P1 channel control signal - P
D9	LA01_N_CC	P1CN	P1 channel control signal -N
D11	LA05_P	FMC_P1CTL1	P1 General Data Port
D12	LA05_N	FMC_P1CTL0	P1 General Data Port
D14	LA09_P	P1D1P	P0 Channel 1 data signal - P

Pin Number	PIN Name	Signal Name	Description
D15	LA09_N	P1D1N	P0 Channel 1 data signal -N
D17	LA13_P	FMC_P1SDA	P1 I2C data
D18	LA13_N	FMC_P1SCL	P1 I2C clock
D20	LA17_P_CC	P0CLKP	P0 channel clock signal - P
D21	LA17_N_CC	P0CLKN	P0 channel clock signal -N
D23	LA23_P	P0D7P	P0 Channel 7 data signal - P
D24	LA23_N	P0D7N	P0 Channel 7 data signal -N
D26	LA26_P	P0D4P	P0 Channel 4 data signal - P
D27	LA26_N	P0D4N	P0 Channel 4 Data Signal -N
G2	CLK1_M2C_P	FMC_I2C_SDA	Data signal connected to the CYUSB4024 dedicated I2C controller
G3	CLK1_M2C_N	FMC_I2C_SCL	Clock signal connected to CYUSB4024 dedicated I2C controller
G6	LA00_P_CC	P1CLKP	P1 channel clock signal - P
G7	LA00_N_CC	P1CLKN	P1 channel clock signal -N
G9	LA03_P	P1D6P	P0 Channel 6 data signal - P
G10	LA03_N	P1D6N	P0 Channel 6 data signal -N
G12	LA08_P	P1D3P	P1 Channel 3 Data Signal - P
G13	LA08_N	P1D3N	P1 Channel 3 Data Signal -N
G15	LA12_P	P1D0P	P1 Channel 0 Data Signal - P
G16	LA12_N	P1D0N	P1 Channel 0 Data Signal - N
G18	LA16_P	FMC_INIT#_RST	INIT interrupt signal
G19	LA16_N	FMC_CDONE	FMC's programming mode OFF indicates that the program is burned to flash via JTAG, and ON indicates that the program is burned via USB.
G21	LA20_P	P0CP	P0 channel control signal - P
G22	LA20_N	P0CN	P0 channel control signal -N
G24	LA22_P	P0D6P	P0 Channel 6 data signal - P
G25	LA22_N	P0D6N	P0 Channel 6 data signal -N
G27	LA25_P	FMC_VBUSDETECTN	VBUS detection signal
G28	LA25_N	FMC_P1CTL4	P1 General Data Port
G30	LA29_P	P0D2P	P0 Channel 2 data signal - P

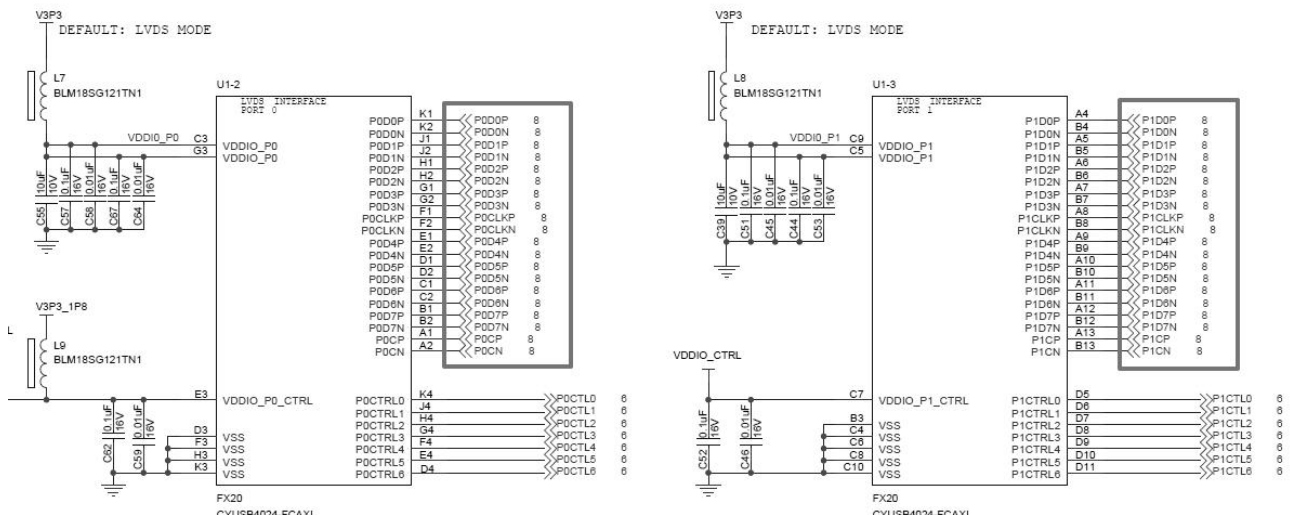
Pin Number	PIN Name	Signal Name	Description
G31	LA29_N	P0D2N	P0 Channel 2 data signal -N
G33	LA31_P	P0D0P	P0 Channel 0 data signal - P
G34	LA31_N	P0D0N	P0 Channel 0 data signal -N
G36	LA33_P	FMC_P0CTL2	P0 General Data Port
G37	LA33_N	FMC_P0CTL3	P0 General Data Port
H4	CLK0_M2C_P	FMC_FX20_RST	Reset signal for CYUSB4024
H5	CLK0_M2C_N	FMC_PMODE	Boot mode selection: High=USB; LOW=SPI FLASH
H7	LA02_P	P1D7P	P1 Channel 7 Data Signal - P
H8	LA02_N	P1D7N	P1 Channel 7 Data Signal -N
H10	LA04_P	P1D5P	P1 5th data signal - P
H11	LA04_N	P1D5N	P1 5th data signal -N
H13	LA07_P	P1D2P	P1 Channel 2 Data Signal - P
H14	LA07_N	P1D2N	P1 Channel 2 Data Signal -N
H16	LA11_P	FMC_P1CTL3	P1 General Data Port
H17	LA11_N	FMC_P1CTL2	P1 General Data Port
H19	LA15_P	FMC_P0SDA	P0 I2C data
H20	LA15_N	FMC_P0SCL	P0 I2C clock
H22	LA19_P	FMC_UART-RTS	fmc uart_rts signal
H23	LA19_N	FMC_UART-CTS	Fmc uart_cts signal
H25	LA21_P	P0D5P	P0 Channel 5 data signal - P
H26	LA21_N	P0D5N	P0 Channel 5 data signal -N
H28	LA24_P	P0D3P	P0 Channel 3 data signal - P
H29	LA24_N	P0D3N	P0 Channel 3 Data Signal -N
H31	LA28_P	P0D1P	P0 Channel 1 data signal - P
H32	LA28_N	P0D1N	P0 Channel 1 data signal -N
H34	LA30_P	FMC_P1CTL5	P1 General Data Port
H35	LA30_N	FMC_P1CTL6	P1 General Data Port
H37	LA32_P	FMC_UART-RX	Dedicated UART controller connected to CYUSB4024
H38	LA32_N	FMC_UART-TX	Dedicated UART controller connected to CYUSB4024

Note: For Ultrascale and Ultrascale+ series FPGA, all LVDS signals of channels P0 and P1 must be connected to the same BANK; the GND signal is not listed in the diagram.

Chapter3 Schematic Analysis and Program Design

3.1 Schematic Analysis

The FL2010 FMC card connects to the FPGA development board via the FMC interface. Its data communication modes include wide link and narrow link. Wide link uses 16 pairs of LVDS differential data transmission; narrow link uses 8 pairs of LVDS differential data transmission. The transmission rate of a single LANE is 594 Mbps in both modes. Data transmission can be implemented using the primitives iserdes3 or bitslip. In the project, primitive control is achieved by instantiating the high_speed_selectio IP core. The schematic diagram of the connection between the CYUSB4024 chip and the FPGA is shown below:



Data signals

P0D0P~P0D7P: 8 pairs of differential data signals for PORT0;

P1D0P~P1D7P: 8 pairs of differential data signals from PORT1;

P0CP and P1CP: Control character input signals; In the DEMO project, the above interfaces are all configured for unidirectional data communication from the FPGA to the CYUSB4024.

Control signals

P0CTL0~P0CTL4: Not used in LVDS mode;

P0CTL5: The link_ready signal sent from CYUSB4024-FCAXI to the FPGA for data link training;

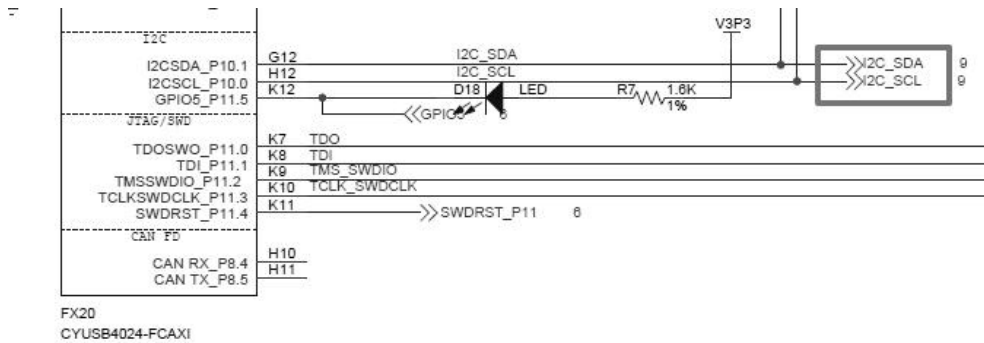
P0CTL6: The buffer_ready signal sent from CYUSB4024 to the FPGA for data transmission control;

The control signal definitions for the P1CTL port are completely identical to those for the P0CTL port.

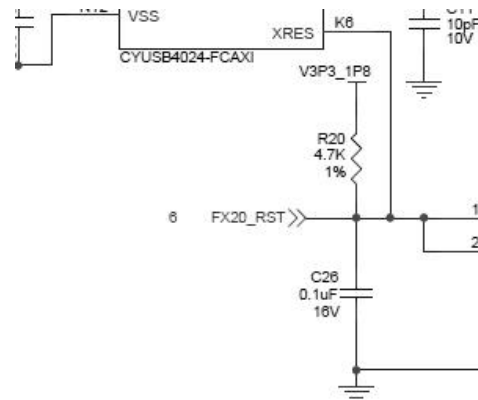
Signal usage rules: When using wide link mode or narrow link with PORT0 selected, use the

P0CTL control signal; when using narrow link with PORT1 selected, use the P1CTL control signal.

In the DEMO project, the FPGA operates as a slave device of the CYUSB4024-FCAXI, and the two communicate via the I2C bus: the FPGA, as an I2C slave, responds to the CYUSB4024's register read and write commands, and the register configuration is determined by the program running on the CYUSB4024-FCAXI side. The locations of the two control signal lines of the I2C bus are shown in the corresponding hardware interface diagram.



When the FL2010 FMC card is powered on, the FPGA provides a low-level reset signal, as shown in the figure:



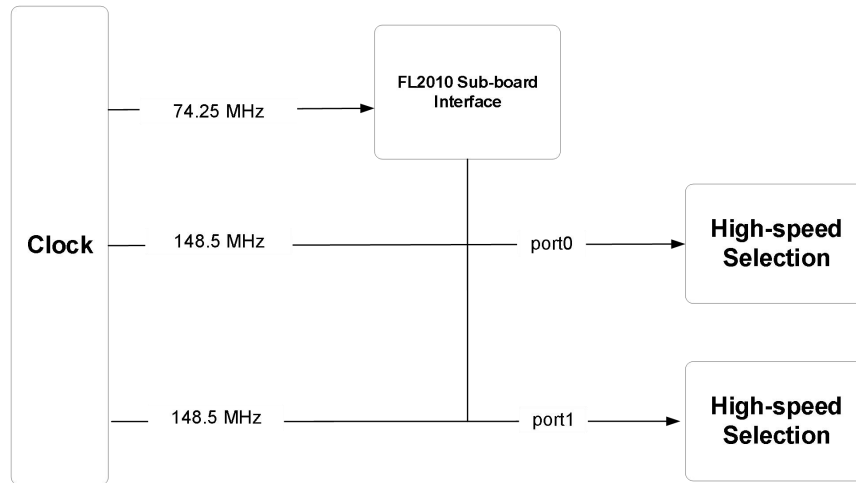
To ensure signal integrity and timing convergence of the high-speed LVDS link, the hardware design must meet the following constraints:

1. All LVDS differential data lines must be connected to the FPGA's HP (High Performance) BANK to meet the electrical and timing requirements of high-speed differential signals;
2. All LVDS differential lines under the same PORT (such as PORT0/PORT1) must be laid out in the same BANK of the FPGA to ensure multi-channel clock phase consistency and normal operation of the link training logic.

3.2 Programming

This FPGA project is divided into three main functional modules: a clock configuration module, an FL2010 interface adaptation module, and an LVDS communication dedicated IP core module. Based on a link line rate of 594 Mbps, the clock is derived, and the system's base clock is configured to be 74.25 MHz. This demo project is built on a Z7_P/Z19 hardware baseboard. In terms of hardware resource allocation, PORT0 is located in FPGA Bank64, and PORT1 is located in FPGA Bank65. Because a single High Speed SelectIO IP can only configure resources in a single

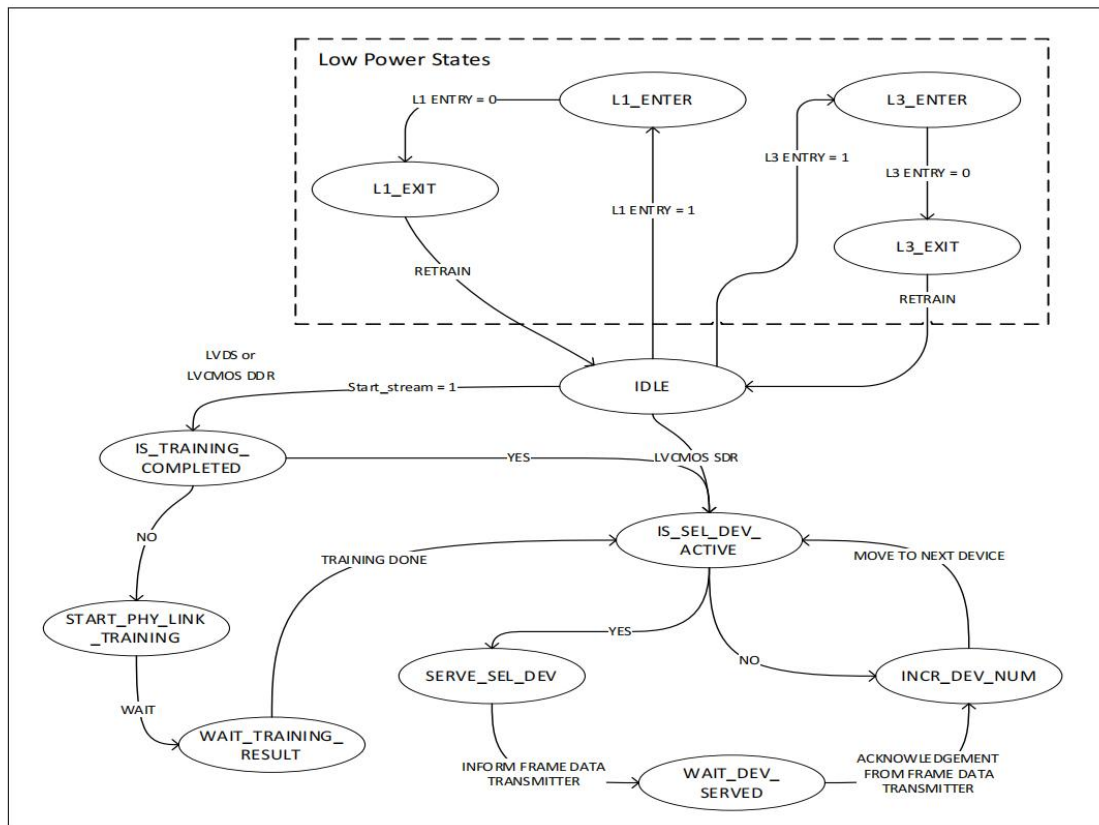
Bank, this project needs to instantiate two independent High Speed SelectIO IP cores to adapt to the LVDS interface resources of Bank64 and Bank65 respectively. The overall project architecture is shown in the figure below.



The FL2010 FMC card interface module is divided into three parts: image generation, I2C slave response simulation, and FL2010 protocol parsing. The image generation unit generates a color bar test image using the `test\_pattern\_generator`, which is then transmitted to the upstream USB 3.2 host device via the FL2010 FMC card simulating camera data flow. The FL2010 protocol parsing unit consists of several low-level control sub-modules, with their specific functions as follows.

- **Device selection DSM**

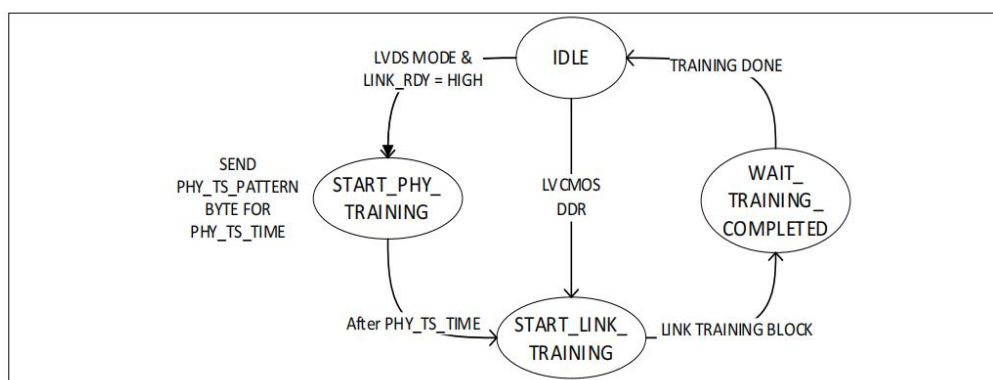
To enable device selection, up to 8 devices can transmit data serially via the LVDS bus. The state machine switching method is shown in the figure.



In low-power mode, no operation is performed. The demo uses LVDS mode. After the project is burned, PHY training is completed first, followed by LINK training. After training is completed, the device traversal state is entered, and the device is traversed in units of frames. The demo only uses one input channel.

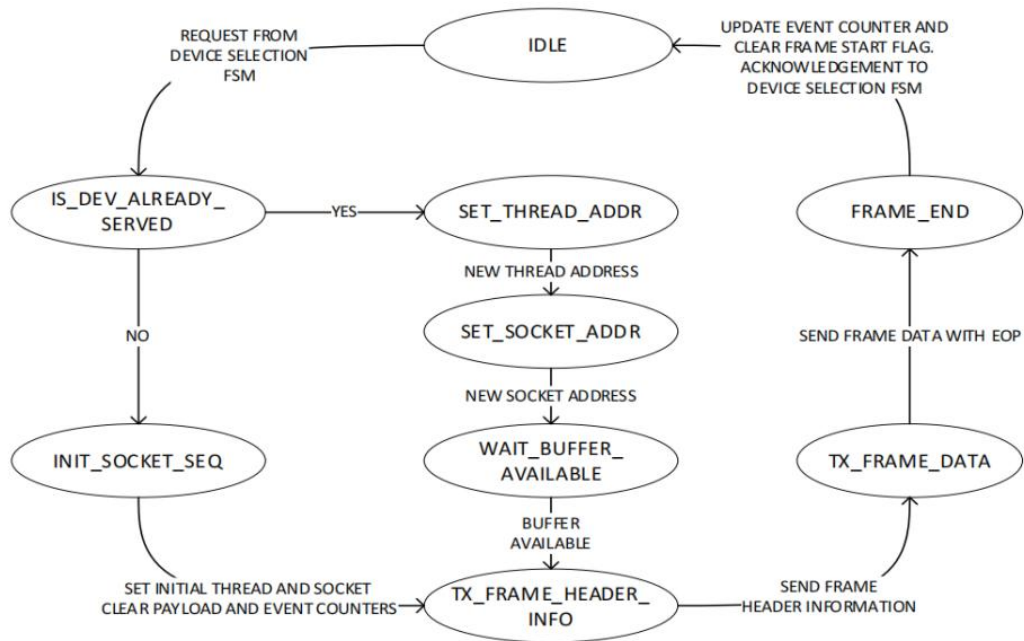
● Phy and link training fsm FSM

This module is used to complete the PHY and LINK training processes. The FL2010 FMC card sends 4 bytes of training configuration data via the I2C interface using register configuration. The module sends the training data sequentially according to a fixed timing order, without waiting for feedback from the FL2010 FMC card. After the training process is completed, the module pushes a training completion indication signal to the FL2010 FMC card via the I2C interface. The overall process is implemented by a state machine scheduler, and the state transition logic is shown in the figure below:



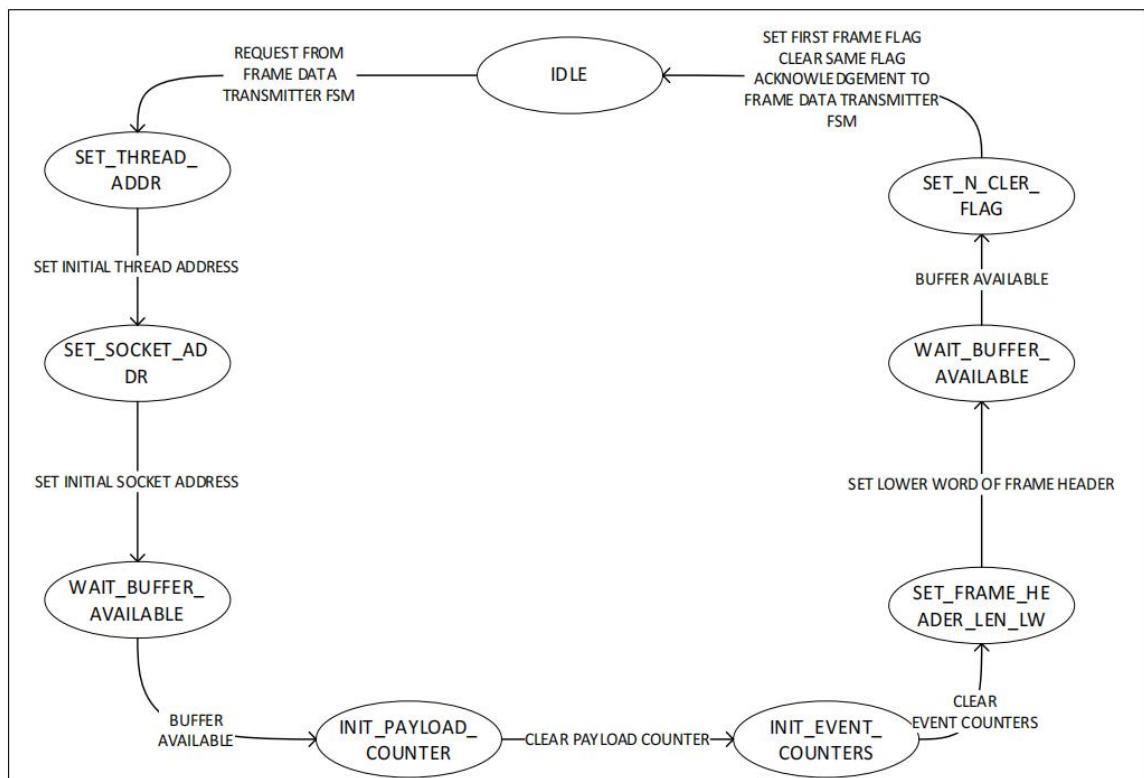
● Frame data transmitter FSM

Used for frame data packaging, the state machine switches after receiving the device serve signal from the dev selection module. Some of these state transitions depend on the FL2010 FMC card firmware configuration.



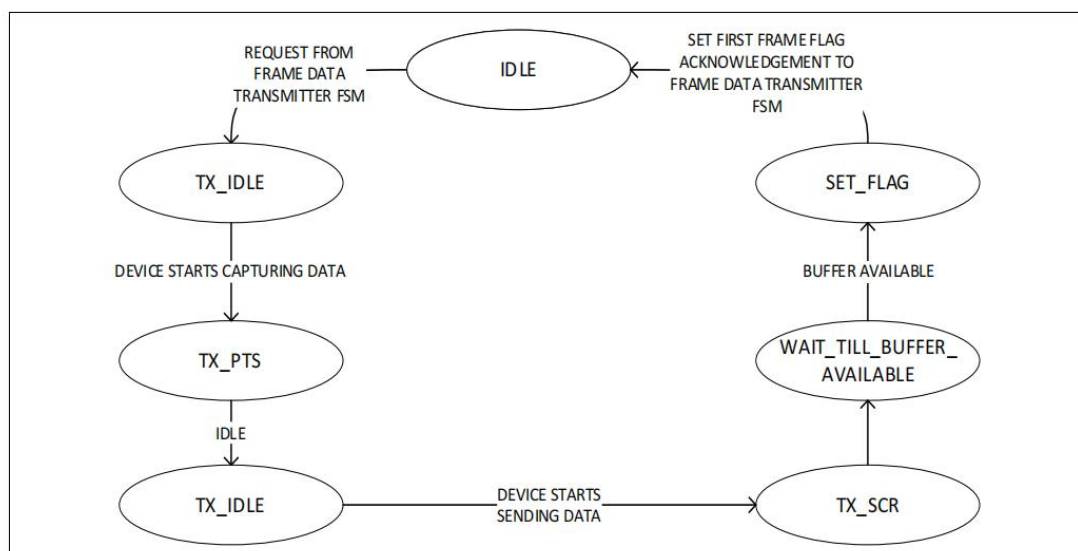
● Initial socket sequence FSM

The initialization order is determined, the thread and socket address are allocated, and the process operates in the `init_socket_seq` state of the Frame data transmitter fsm. The state machine switching method is shown in the figure:



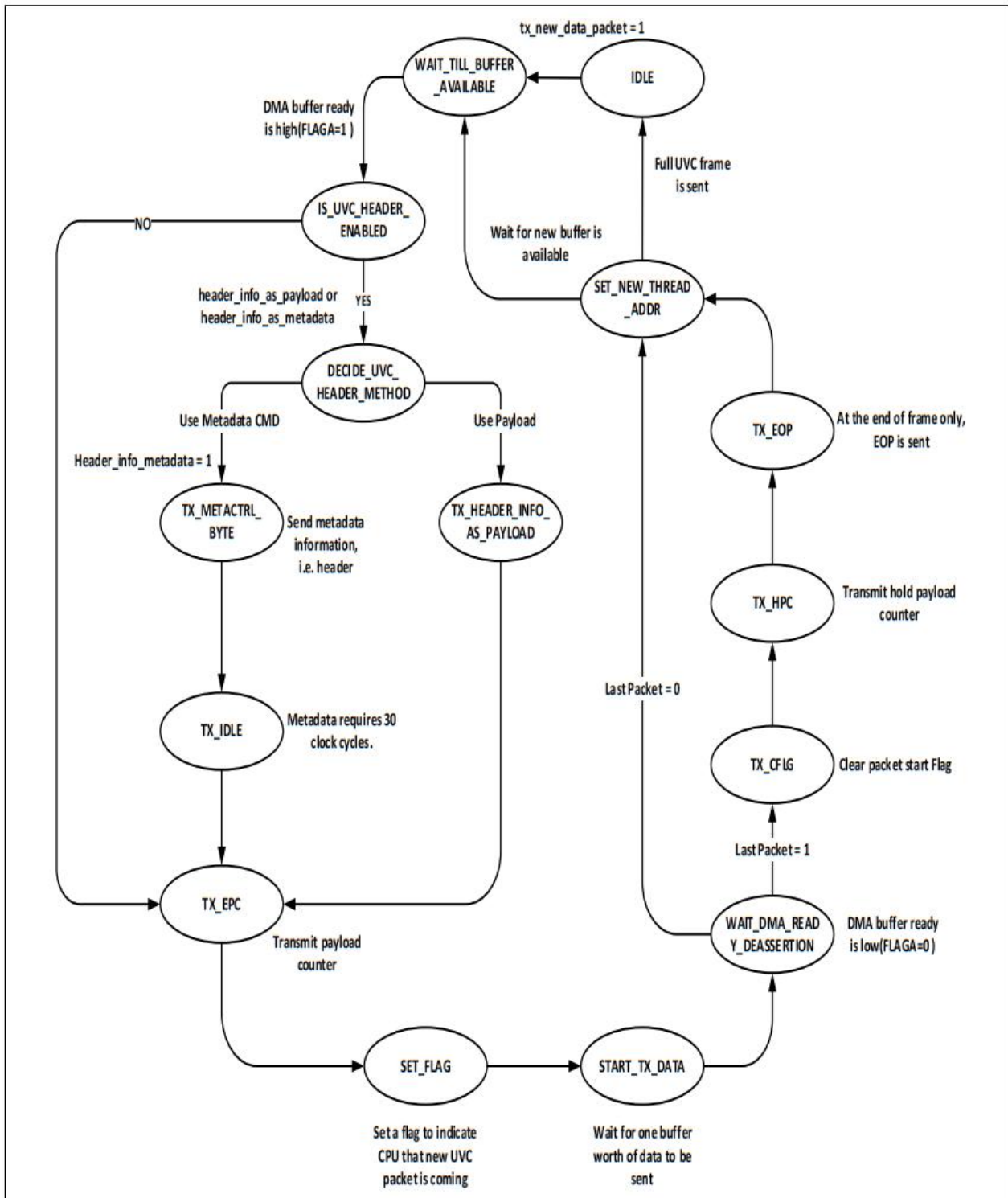
● Frame header transmitter FSM

Configure the frame header heuristic information. This process begins after the Frame data transmitter FSM enters TX_FRAME_HEADER_INFO. The state machine switching method is shown in the figure.



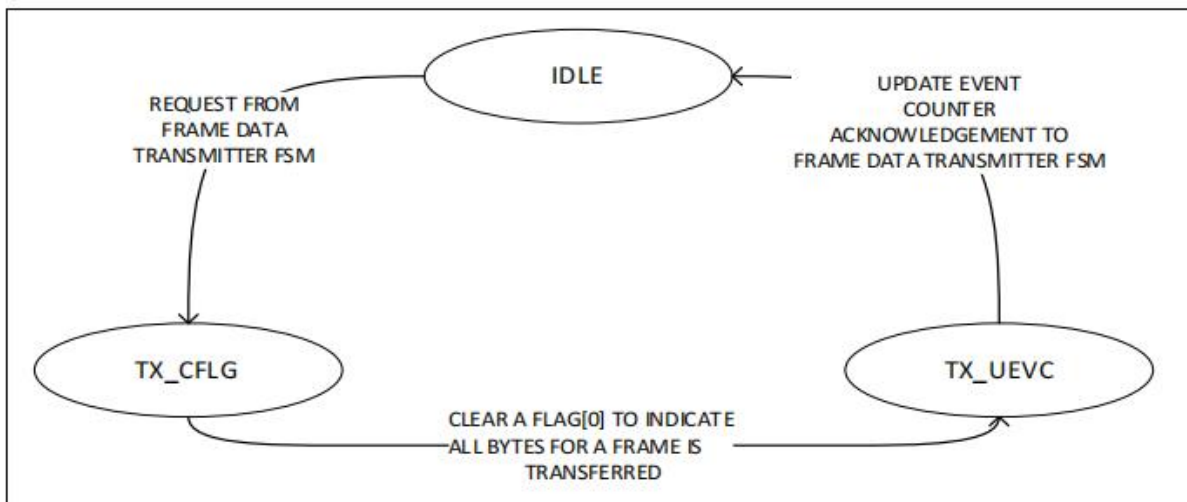
● LVDS data packet transmitter FSM

The state machine is shown in the figure, which implements the data packet transmission function.



- Frame end seq FSM

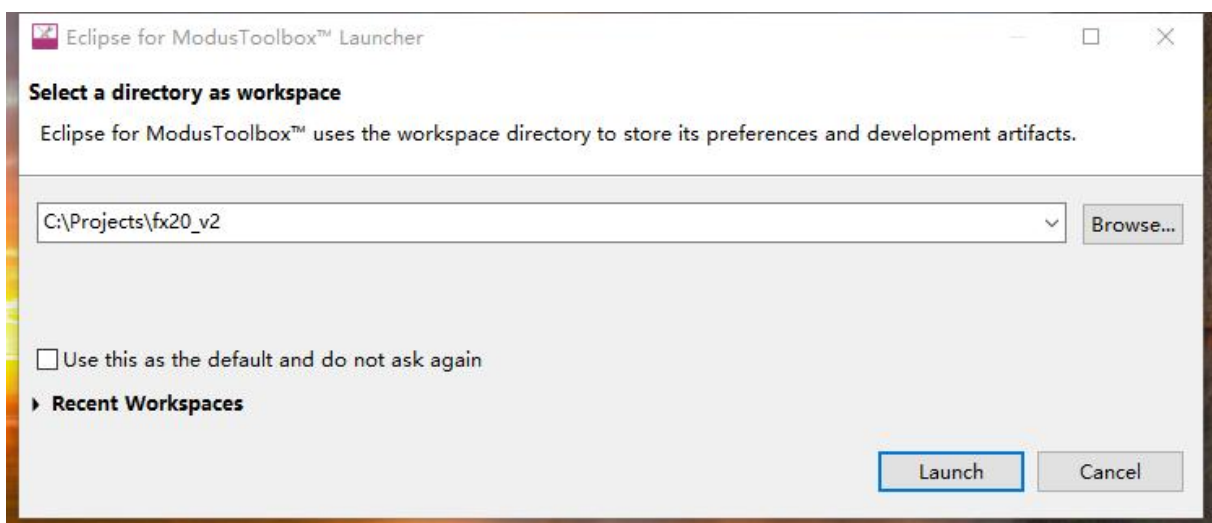
At the end of each frame, an end-of-frame signal must be sent, and the state machine transition is shown in the figure.



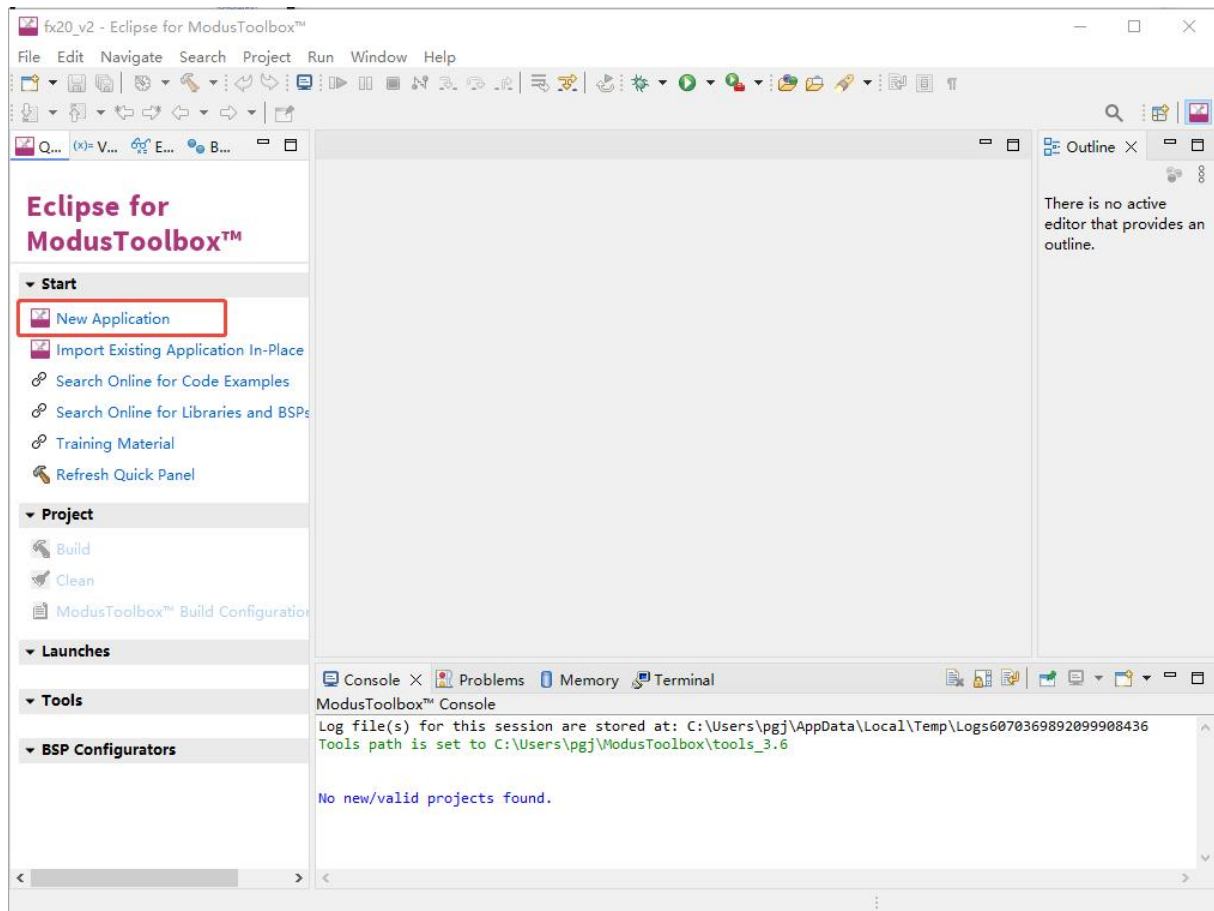
Chapter4 Firmware

Users can re-flash the firmware of CYUSB4024 using the following steps. First, the firmware should be compiled according to the following steps.

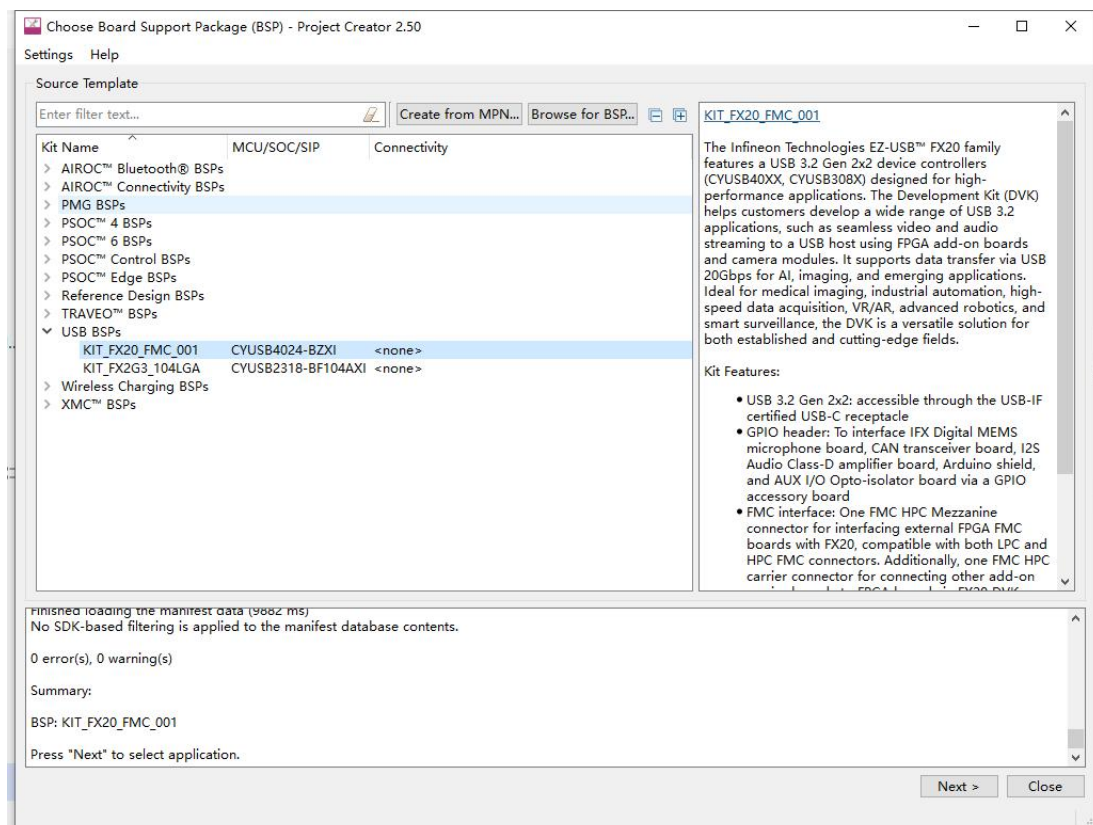
- 1) Open Eclipse and select workspace



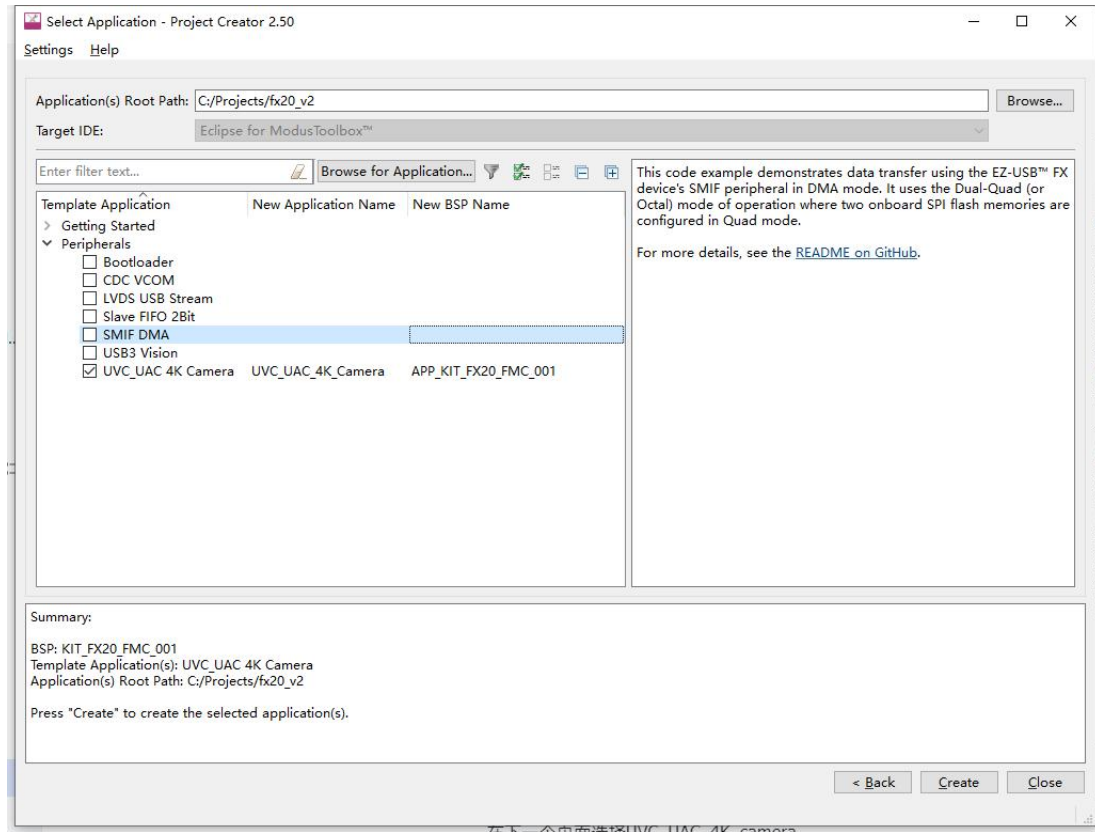
- 2) Select New Application



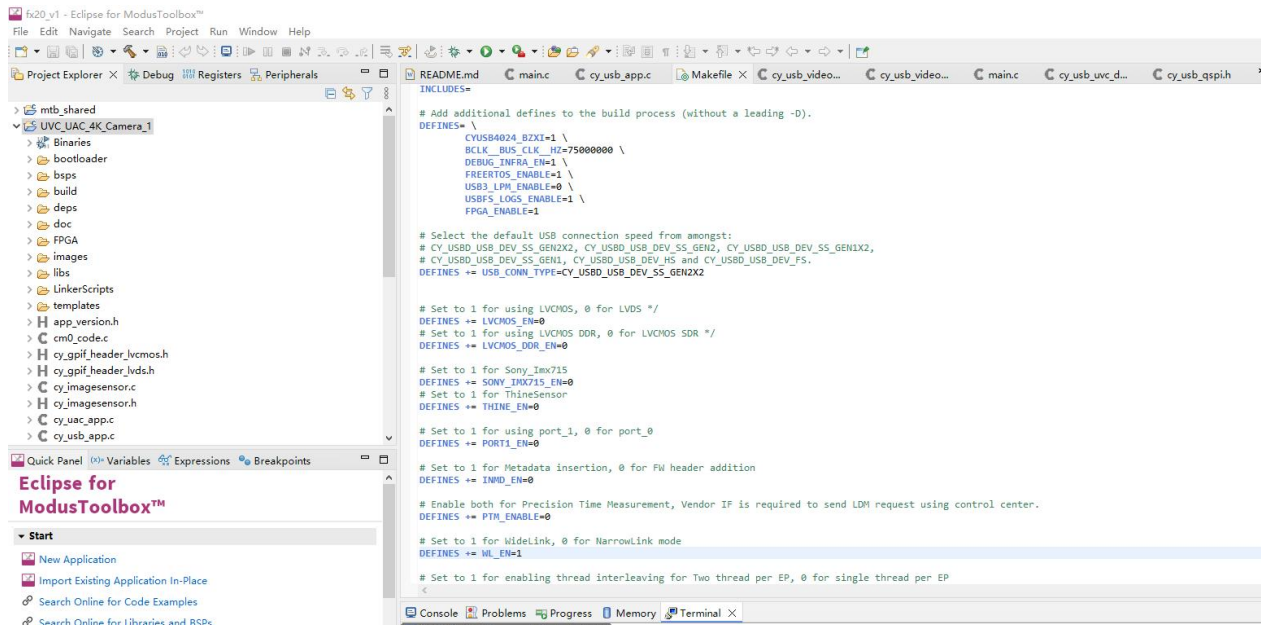
3) Here, select FX20 for BSP.



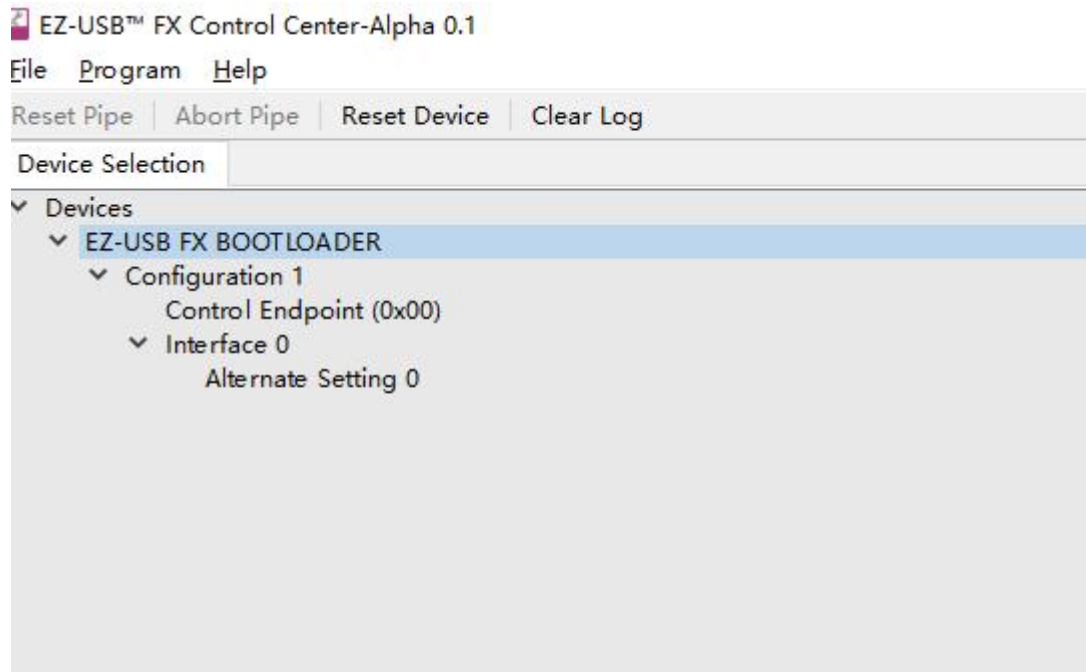
4) On the next page, select UVC_UAC_4K_camera



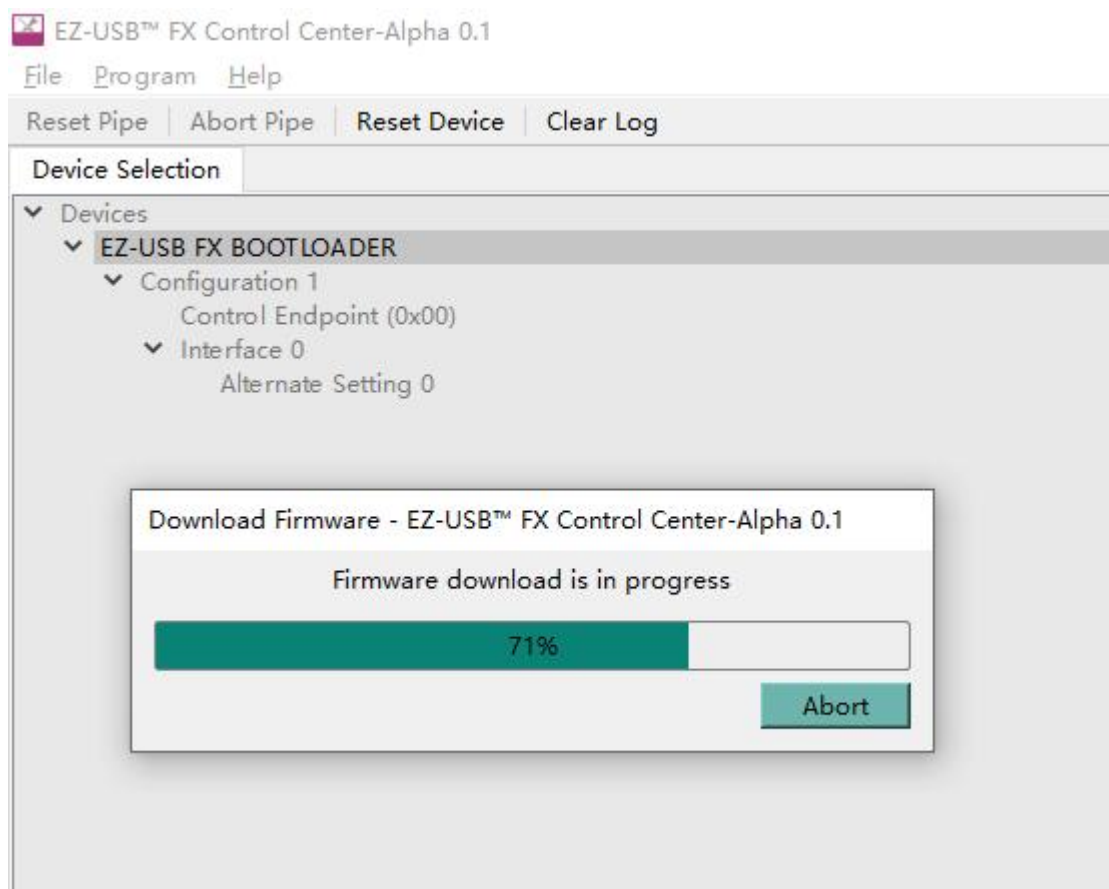
- 5) Open the Makefile in this interface. WL_EN = 1 indicates that wide link mode is enabled, and port1_en is set to 0 in this case.



- 6) Connect the module to the computer motherboard with the jumper cap set to USB power mode. After the LED lights up, press key 1 (reset button), then press key 2 (boot mode button) without releasing it. When releasing, release key 1 first, then key 2. The following screen will be displayed in the EZ-USB FX Control Center.



- 7) Select Program -> Internal Flash, then select the .hex file in the project path to burn the program.



Because the internal flash memory has a limited capacity, the size of the HEX file cannot exceed the internal flash memory size. The log below indicates whether the process was successful.

```
Log
BL is active
Internal flash firmware program file is -> C:/Projects/fx20_v1/UVC_UAC_4K_Camera_1/build/APP_KIT_FX20_FMC_001/Release/mtb-example-f
Download firmware...
Firmware downloading is complete
Reset device

Reset device successful
Firmware download is successful
\\?\USB#VID_04B4&PID_00E1#01AF160B03911C7C#{01234567-2a4f-49ee-8dd3-fadea377234a}
Device detached : \\?\USB#VID_04B4&PID_00E1#01AF160B03911C7C#{01234567-2a4f-49ee-8dd3-fadea377234a}
\\?\USB#VID_04B4&PID_00E1#01AF160B03911C7C#{01234567-2a4f-49ee-8dd3-fadea377234a}
Device attached : \\?\USB#VID_04B4&PID_00E1#01AF160B03911C7C#{01234567-2a4f-49ee-8dd3-fadea377234a}
BL is active
External SPI flash programming is active
Internal flash firmware program file is -> C:/Projects/fx20_v1/UVC_UAC_4K_Camera_1/build/APP_KIT_FX20_FMC_001/Release/mtb-example-f
Download firmware...
Firmware downloading is complete
Reset device

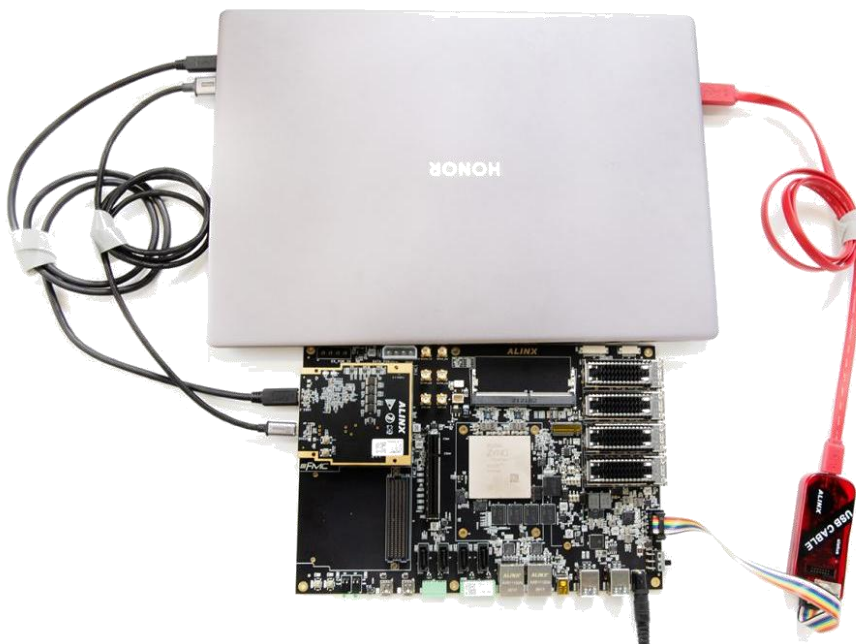
Reset device successful
Firmware download is successful
\\?\USB#VID_04B4&PID_00E1#01AF160B03911C7C#{01234567-2a4f-49ee-8dd3-fadea377234a}
Device detached : \\?\USB#VID_04B4&PID_00E1#01AF160B03911C7C#{01234567-2a4f-49ee-8dd3-fadea377234a}
```

All factory-installed boards come with pre-programmed firmware, with a default resolution of 4K. The boards also support multiple resolutions such as 720p and 1080p.

Chapter5 Module Connection and Debugging

5.1 Module Connection

The FL2010 module and FPGA development board are directly connected via the FMC interface and secured with screws. The module's USB 3.2 interface connects to the host computer's USB 3.2 interface, and the DEBUG debugging interface connects to the host computer's USB 2.0 interface. The hardware connection between the Z19 development board and the FL2010 module's FMC is shown in the following figure :



After the system powers on, two LED light up, indicating that the hardware is in a reset state; the reset signal is connected to the FPGA chip pin. When the baseboard is powered on but the

FPGA program has not been programmed, the CYUSB4024 has no serial port output; after the FPGA program is programmed, the serial port will output log information.

5.2 Frequently Asked Questions

When the serial port log shows error messages, it indicates that the data transmission link has been abnormally interrupted. First, check the board's hardware connection status, or reprogram the FPGA project. If the fault persists, it can be categorized into two normal operating conditions:

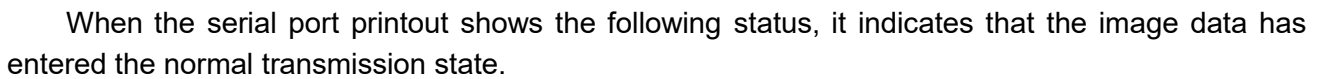
1. The FPGA is working in debug mode. The link training has been completed, but image data transmission has not been started.
2. The camera application software is not running on the USB 3.2 host computer.

```
Info:APP:UVC Class Requests
Info:APP:CY_USB_CTRL_REQ_RECIPENT_INTF && CY_USB_UVC_INTERFACE_VS = 0x1
Info:APP:UVC_GET_CUR_DEF_MIN_MAX_REQ:81
Info:APP:isReqHandled = 1
Info:APP:AppSetupCallback

Info:APP:UVC Class Requests
Info:APP:CY_USB_CTRL_REQ_RECIPENT_INTF && CY_USB_UVC_INTERFACE_VS = 0x1
Info:APP:CY_USB_UVC_SET_CUR_REQ
Info:APP:isReqHandled = 1
Info:APP:CY_USB_UVC_DEVICE_SET_CUR_RQT
Info:APP:queueMsg.data[0] = 34
Info:APP:UVC_SET_CUR_REQ wValue = 0x100 wIndex = 0x1
Info:APP:AppSetupCallback

Info:APP:UVC Class Requests
Info:APP:CY_USB_CTRL_REQ_RECIPENT_INTF && CY_USB_UVC_INTERFACE_VS = 0x1
InegAddr=0x20, Data=0x0
Info:APP:i2c status = 0x0
Info:APP:Video App = 0
Info:APP:format_index 1 resolution_index 1 devSpeed = 6
Info:APP:I2cWrite SlaveID=0xD, RegAddr=0x2B, Data=0x0
Info:APP:I2cWrite SlaveID=0xD, RegAddr=0x27, Data=0x10
Info:APP:I2cWrite SlaveID=0xD, RegAddr=0x25, Data=0xF
Info:APP:I2cWrite SlaveID=0xD, RegAddr=0x24, Data=0x0
Info:APP:i2c status = 0x0 IMAGE_WIDTH :3840
Info:APP:I2cWrite SlaveID=0xD, RegAddr=0x23, Data=0x8
Info:APP:I2cWrite SlaveID=0xD, RegAddr=0x22, Data=0x70
Info:APP:i2c status = 0x0 IMAGE_HIGHT :2160
Info:APP:I2cWrite SlaveID=0xD, RegAddr=0x21, Data=0x0
Info:APP:I2cWrite SlaveID=0xD, RegAddr=0x26, Data=0x3C
Info:APP:i2c status = 0x0 FPS :60
Info:APP:Cy_LVDS_GpifsMSwitch line 1291
Info:APP:I2cWrite SlaveID=0xD, RegAddr=0x20, Data=0x2
Info:APP:i2c status = 0x0
Info:APP:Video App = 1
FPGA Configuration failed..Check troubleshooting section of user guide
FPGA Configuration failed..Check troubleshooting section of user guide
FPGA Configuration failed..Check troubleshooting section of user guide
```

After the host computer opens the camera software, the interface will display as shown in the following image:



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